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Organic field-effect transistors and all-polymer integrated circuits

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Abstract

Electrical properties of field-effect transistors made of different solution processable organic semiconductors are described. The temperature and gate-voltage dependence of the mobility is shown and theoretically described using a model based on the variable-range hopping of charge carriers in an exponential density of states. Furthermore, a technology has been developed to make all-polymer integrated circuits. It involves reproducible fabrication of field-effect transistors on flexible substrates, where the semiconducting, conducting and insulating parts are all made of polymers. Integrated circuits consisting of more than 300 field-effect transistors are demonstrated. © 1999 Elsevier Science B.V. All rights reserved.

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1. Introduction

In recent years the use of organic semiconductors in field-effect transistors has gained considerable interest due to their potential application in low-cost integrated circuits or as thin-film transistors in active matrix LCD displays. Most effort has been put into increasing the hole mobility of the semiconductor and increasing the on-off ratio of the field-effect transistor by optimising existing materials and by applying new materials. Mobilities as high as $2 \text{ cm}^2/\text{V s}$ and on-off ratios of 108 have recently been reported in thin-film transistors of evaporated pentacene [1,2]. Furthermore, attention has been focused on the improvement of

the processability of these materials by using directly soluble [3] or precursor organic semiconductors [4]. Easy processing is a prerequisite for the development of low-cost plastic electronics that can compete with silicon on the low-end market. This may also mean that the (organic) semiconductor is only a part of a complete integrated-circuit technology that is potentially cheap in total. Furthermore, the interesting property of mechanical flexibility can only be exploited if the organic semiconductor is used in a flexible environment. The combination of materials research and integration technology is the subject of this paper.

The paper is organized as follows. First the electrical transport properties of two solution-processable organic semiconductors, a polymer (polythiénylenevinylene, PTV) and a small molecule (pentacene), are investigated, by describing

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and modeling the temperature dependence of the field-effect mobility. Secondly, it is shown that the room temperature mobility of these semiconductors can be improved by optimising the process conditions. Finally, a technology is described to make all-polymer integrated circuits. Functional integrated circuits of more than 300 transistors are demonstrated.

2. Electrical transport in amorphous organic semiconductors

Besides the technical applicability of organic semiconductors, their electronic and structural properties have been the subject of investigation as well. Interesting questions like the connection between molecular order and hole mobility in conjugated oligomers and polymers have been addressed [1,8–11].

Experiments have indicated that the field-effect mobility of holes in organic transistors depends on the temperature as well as on the applied gate bias [4,12]. This has been described by Horowitz et al. [12] using a multiple trapping and release model. In this model the assumption is made that most of the charge carriers are trapped in localized states. Then the amount of (temporarily) released charge carriers to an extended-state transport level (the valence band for classical p-type semiconductors) depends on the energy level of the localized states, the temperature, and the gate voltage. However, while extended-state transport may occur in highly ordered vacuum-evaporated molecular films [12] it is not expected to play a role in amorphous organic films [4] where the charge carriers are strongly localized.

Here a theory for the field-effect mobility in amorphous organic transistors is described, where the charge transport is governed by hopping, i.e. the thermally activated tunneling of carriers between localized states, rather than by the activation of carriers to an extended-state transport level. The concept of variable range hopping (VRH) is used, i.e. a carrier may either hop over a small distance with a high activation energy or hop over a long distance with a low activation energy. In a field-effect transistor, an applied gate voltage

gives rise to the accumulation of charge in the region of the semiconducting layer that is close to the insulator. As these accumulated charge carriers fill the lower-lying states of the organic semiconductor, any additional charges in the accumulation layer will occupy states at relatively high energies. Consequently, these additional charges will (on average) require less activation energy to hop away to a neighboring site. This results in a higher mobility with increasing gate voltage. The influence of temperature and the influence of the filling of states on the conductivity is studied in a VRH system with an exponential distribution of localized-state energies. Using percolation theory, an analytic expression is derived for the conductivity. This expression is then used to derive the field-effect mobility of the carriers when the material is applied in a transistor. Finally, the result is used to interpret the experimentally observed temperature and gate-voltage dependence of the field-effect mobility in both a pentacene and a polythiophene vinylene (PTV) organic thin-film transistor [4]. Here, only the main results of the calculation are given, for a full derivation see Ref. [13]. First an expression is derived for the conductivity as a function of temperature T and charge carrier density. At low carrier densities and low T , the transport properties are determined by the tail of the density of (localized) states (DOS), which is modeled by

$$g(\varepsilon) = \frac{N_t}{k_B T_0} \exp\left(\frac{\varepsilon}{k_B T_0}\right) \quad (-\infty < \varepsilon \leq 0), \quad (1)$$

where N_t is the number of states per unit volume, k_B is Boltzmann's constant, and T_0 is a parameter that indicates the width of the exponential distribution. The density of states $g(\varepsilon) = 0$ for positive values of ε . Let the system be filled with charge carriers, such that a fraction $\delta \in [0,1]$ of the localized states is occupied by a carrier, i.e. such that the density of charge carriers is δN_t . In equilibrium, the energy distribution of the carriers is given by the Fermi–Dirac distribution $f(\varepsilon, \varepsilon_F)$, where ε_F is the Fermi energy (or chemical potential). For a given carrier occupation δ the position of the Fermi energy ε_F is fixed by the condition

$$\delta = \frac{1}{N_t} \int d\varepsilon g(\varepsilon) f(\varepsilon, \varepsilon_F) \approx \exp\left(\frac{\varepsilon_F}{k_B T_0}\right) \Gamma(1 - T/T_0) \Gamma(1 + T/T_0), \quad (2)$$

where $\Gamma \equiv \int_0^\infty \exp(-y)y^{z-1}$. In Eq. (2) the assumption is made that most carriers occupy the sites with energies $\varepsilon \ll 0$ i.e., $-\varepsilon_F \gg k_B T_0$. This condition is fulfilled when δ and T are low. Note that at $T=0$ the gamma functions are unity and the carrier density is given by the density of states with energies lower than ε_F . The approximate expression (2) breaks down at temperatures $T \geq T_0$, since most carriers are then located close to $\varepsilon=0$.

The transport of carriers is governed by the hopping of carriers between localized states, which is strongly dependent on the hopping distances as well as the energy distribution of the states. At low bias, the system can be described as a resistor network [14,15]. Based on percolation theory [15–17] an expression has been derived for the conductivity σ as a function of the occupation δ and the temperature T [13]:

$$\sigma(\delta, T) = \sigma_0 \left(\frac{\pi N_t \delta (T_0/T)^3}{(2\alpha)^3 B_c \Gamma(1 - T/T_0) \Gamma(1 + T/T_0)} \right)^{T_0/T}, \quad (3)$$

where σ_0 is a (unknown) prefactor, α is an effective overlap parameter, which governs the tunneling process between two localized states, and $B_c \cong 2.8$ is the critical number of bonds per site in the percolating network [16,17].

Note that the conductivity has an Arrhenius-like temperature dependence $\sigma \sim \exp[-E_a/(k_B T)]$, with an activation energy E_a that is weakly (logarithmically) temperature dependent. This is in strong contrast with the well-known Mott formula for VRH in a constant DOS, where $\sigma \sim \exp[(-T_1/T)^{1/4}]$ [18]. The temperature dependence of the Mott formula is a consequence of hopping over far distances and hopping to high energies being equally important. In an exponential DOS, however, the characteristic hop is an

activated jump, since there are much more available states at higher energies.

Now the obtained conductivity (3) is applied to describe the field-effect mobility μ_{FE} in a transistor. In bulk material, the mobility μ of the charge carriers is given by $\mu = \sigma(\delta, T)/(e\delta N_t)$. In a transistor, however, the charge density is not uniform, but it decreases with the distance x from the semiconductor-insulator interface. According to Eq. (2), the occupation $\delta(x)$ depends on the distance x through the gate-induced potential $V(x)$,

$$\delta(x) = \delta_0 \exp\left(\frac{eV(x)}{k_B T_0}\right), \quad (4)$$

where δ_0 is the carrier occupation far from the semiconductor-insulator interface, where $V(x) = 0$. The variations of $V(x)$ and $\delta(x)$ with the distance x are determined by the Poisson equation. Substituting the distance-dependent charge occupation $\delta(x)$ into Eq. (3) for the conductivity, the source-drain current of the transistor in the linear regime ($-V_D < -V_G$) reads

$$I = \frac{WV_D}{L} \int_0^t dx \sigma[\delta(x), T]. \quad (5)$$

Here, V_D is the drain voltage (the source is the ground electrode) and L , W and t are the length, width, and thickness of the channel, respectively. The field-effect mobility then follows from the transconductance (see, e.g., Ref. [4])

$$\mu_{FE} \equiv \frac{L}{C_i W V_D} \frac{\partial I}{\partial V_G}. \quad (6)$$

From Eqs. (3)–(6) the following expression is obtained for the field-effect mobility [13],

$$\mu_{FE} = \frac{\sigma_0}{e} \left(\frac{\pi (T_0/T)^3}{(2\alpha)^3 B_c \Gamma(1 - T/T_0) \Gamma(1 + T/T_0)} \right)^{T_0/T} \times \left[\frac{(C_i V_G)^2}{2k_B T_0 e_s} \right]^{T_0/T-1}, \quad (7)$$

where the assumption is made that the thickness t of the semiconductor layer is sufficiently large such that $V(t)=0$. Then the field-effect mobility is independent of the thickness t as well as the bulk carrier occupation q_0 .

The result (7) is applied to the experimental data of Ref. [4], where the drain current I versus gate voltage V_G characteristics have been measured of both a pentacene and a polythiénylene vinylene (PTV) organic thin-film transistor at a range of temperatures. The precursors of both organic semiconductors are spin-coated from solution on a substrate consisting of a heavily n -doped silicon (common) gate electrode, a 200 nm thick SiO_2 insulating layer ($C_i = 17 \text{ nF cm}^{-2}$) and a patterned gold layer as the source and drain electrodes. The precursors are converted into the organic semiconductors using a process described in Ref. [4]. Typical channel widths and lengths were $W = 10\text{--}20 \text{ mm}$ and $L = 2\text{--}20 \text{ }\mu\text{m}$, respectively. The film thickness t varied from 30 to 50 nm. For both semiconductors, a relative dielectric constant $\epsilon_r = 3$ is used, which is appropriate for most organic solids. In Fig. 1 the field-effect mobility in a pentacene and in a PTV thin-film transistor is plotted against the inverse temperature for different gate voltages. Experimentally, the field-effect mobilities are determined from Eq. (6) at $V_D = -2 \text{ V}$. The theoretical curves (solid lines) follow from Eq. (7), where σ_0 , α , and T_0 are used as fitting parameters. The agreement with experiment is quite good (the parameter values are given in Table 1). The

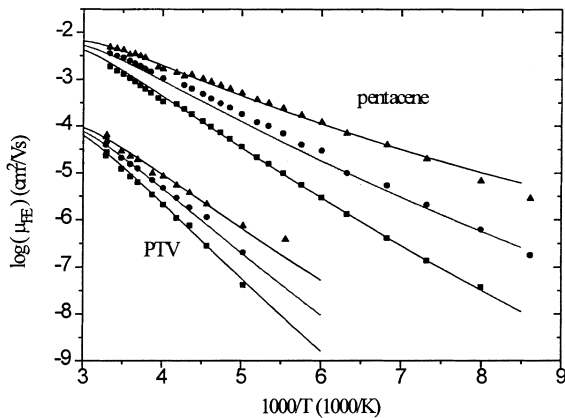


Fig. 1. Field-effect mobility μ_{FE} in a pentacene and a polythiénylene vinylene (PTV) thin-film transistor as a function of temperature T for different gate voltages $V_G = -20 \text{ V}$ (triangles), -10 V (circles) and -5 V (squares). The experimental data (symbols) are taken from Ref. [4]. The solid lines are according to Eq. (7), using the parameters given in Table 1.

Table 1

The pre-exponential factor to the conductivity σ_0 , the overlap parameter α^{-1} and the width of the exponential distribution of localized states T_0 for both pentacene and polythiénylene vinylene (PTV) as obtained from the fit of Eq. (7) to the experimental data of [4], see Fig. 1

	σ_0 (10^{10} S/m)	α^{-1} (Å)	T_0 (K)
Pentacene	1.6	2.2	385
PTV	0.7	0.8	380

temperature dependence of μ_{FE} , as shown in Fig. 1, follows a simple Arrhenius behavior $\mu_{\text{FE}} \sim \exp[-E_a/(k_B T)]$, where the activation energy E_a depends on V_G as plotted in Fig. 2. The decrease of E_a with increasing (negative) gate voltage is the direct result of accumulated charges filling the lower-lying states.

The field-effect mobility in PTV is more than two orders of magnitude lower than the field-effect mobility in pentacene. Furthermore, the activation energy for PTV is about twice the activation energy for pentacene. Surprisingly, these differences cannot be attributed to differences in the prefactor σ_0 nor to the width of the energy distribution T_0 , as these parameters have similar values for PTV as well as pentacene (see Table 1). The main difference between pentacene and PTV appears to be in the overlap parameter α , which determines the tunneling process between different sites. Note that this key parameter is absent in a multiple-trapping

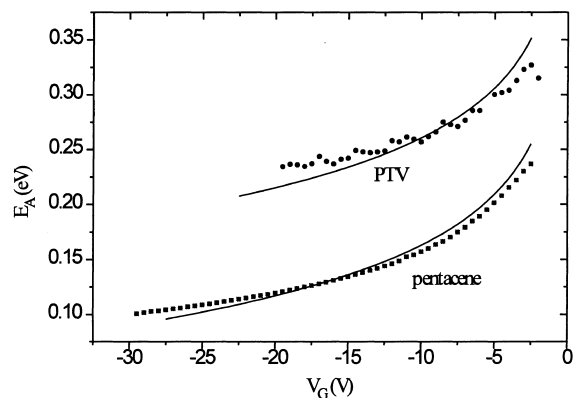


Fig. 2. Activation energy E_a for the field-effect mobility in a pentacene and a polythiénylene vinylene (PTV) thin-film transistor as a function of the gate voltage V_G . The experimental data (squares) are taken from Ref. [4]. The solid lines are calculated from Eq. (7), using the parameters given in Table 1.

model, where the transport is governed by thermal activation from traps to a conduction band and subsequent retrapping, without involving a tunneling step. As the length scale α^{-1} is smaller than the size of a molecule, one must be cautious not to interpret α^{-1} simply as the decay length of the electronic wave function. The size and shape of the molecules and the morphology of the organic film are expected to have an important influence on the tunneling probability as well. The observed difference in α^{-1} may be due to the fact that there is more steric hindrance in the polymer PTV than in a system of small pentacene molecules. The better stacking properties of pentacene give rise to a larger area of overlap of the electronic wave functions, which results in a larger effective overlap α^{-1} in the model. Hence in the solution-processed organic transistors discussed here, the field-effect mobility appears to be limited by the structural order of the organic semiconducting layer.

3. Improved processing of precursor organic semiconductors

As explained in the previous section the mobility of organic semiconductors depends on the ordering of the material. As a consequence it is worthwhile trying to optimize the ordering in the thin films by varying the process parameters, for example the conversion conditions of the precursor materials. Furthermore, the main part of the electrical transport in the thin-film transistors takes place in the first few nanometers of the film at the semiconductor insulator interface. Improving the interface can also lead to a better performance of the transistor. While the (microscopic) mechanisms are still subject of investigation, the mobility of the precursor-route pentacene transistors was improved by more than one order of magnitude to $0.1 \text{ cm}^2/\text{V s}$ [19]. This was achieved by converting the precursor on a hot plate at 200°C for 5 s, different from the conditions used earlier [4]. Also the SiO_2 surface was treated with the hydrophobic primer hexamethyldisilazane (HMDS). The conversion of precursor PTV on a primed SiO_2 surface also led to a higher mobility ($0.001 \text{ cm}^2/\text{V s}$) compared to previous results [4].

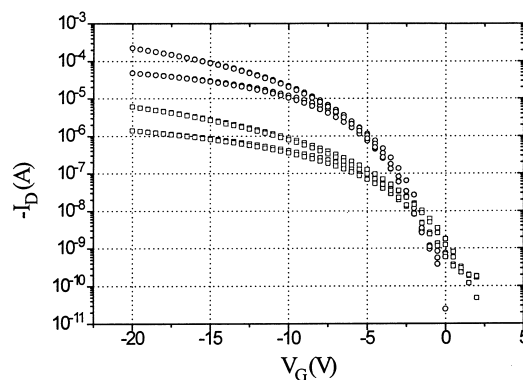


Fig. 3. Drain current versus gate voltage taken at drain voltages of -2 V (bottom curve) and -20 V (top curve) for both a pentacene (circles) a PTV (squares) thin film transistor. The capacitance of the insulator is 17 nF/cm^2 , the channel width over length ratio is 1000.

The transfer characteristics of both a pentacene and a PTV thin-film transistor are shown in Fig. 3. The temperature and gate-voltage dependence of the mobility of these improved transistors is under investigation. However, it is interesting to note that the high mobility of the pentacene transistors is only one order of magnitude lower than the mobility of the pentacene transistors prepared by thermal evaporation under controlled conditions [1,2].

4. All-polymer integrated circuits

As discussed in the previous section, organic semiconductors have been applied as the active component in thin film transistors. Charge carrier mobilities comparable to that of amorphous silicon ($0.1 \text{ cm}^2/\text{V s}$) were obtained [1–3]. Organic transistors have also been combined [4] into logic gates. However, with a few exceptions [20], only the semiconductor consisted of an organic material. The other parts of the field-effect transistors, namely source, drain and gate electrode, and gate dielectric, were made with standard lithographic and etching techniques of conventional inorganic materials. Recently, we have developed a technology that makes it possible to fabricate all-polymer transistors that can be combined into all-polymer integrated circuits. A summary of our

results is given below. A more detailed description is given in Refs. [5–7].

In order to fabricate the conducting parts of the all-polymer integrated circuits use is made of photo-chemically patterning [21] of doped polyaniline (PANI) conducting films as shown in Fig. 4. A micrograph of a structured PANI film is also displayed.

Polyaniline p-doped with camphorsulfonic acid is dissolved [22] in m-cresol. A photoinitiator is

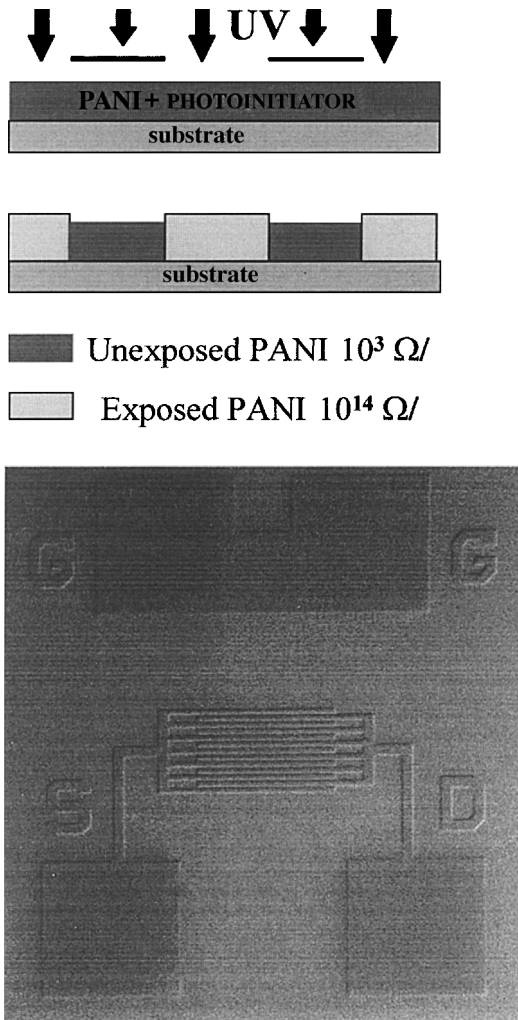


Fig. 4. (a) Patterning of a conducting polyaniline film using deep UV light through a mask. (b) Micrograph of a structured polyaniline film. Shown here are the (interdigitated) source and drain contacts of a single all-polymer transistor.

added to this solution which is then spin-coated onto a substrate such as a polyimide foil. Under a nitrogen atmosphere the film is exposed through a mask to deep UV radiation. Upon exposure the conducting polyaniline is reduced to the nonconducting form. The sheet resistance then increases from $103 \Omega/\square$ to more than $10^{14} \Omega/\square$. As a result, conducting tracks are embedded in an otherwise insulating film. The height differences between the exposed and unexposed parts of the film, with thickness typically $0.2 \mu\text{m}$, is less than 50 nm and thus no further planarisation is necessary. Unexposed photoinitiator is removed through sublimation by heating at 110°C .

The conducting PANI tracks are used as interconnects and as terminals of all-polymer field-effect transistors.

A cross section of the discrete PMOS transistors is shown schematically in Fig. 5. Only three masks are needed in the process. A polyimide foil glued onto a carrier, e.g. currently a regular silicon wafer, is used as a substrate. The source and drain electrodes are defined in the bottom PANI layer by UV light exposure through the first mask. Then a 50 nm thin semiconducting [4] polythiylenevinylene (PTV) film is applied by conversion of a spincoated precursor film. The PTV film largely determines the electrical parameters of the transistor. It is noted that PTV is not a state-of-the-art organic semiconductor, it is being used only to optimize the technology. Onto the PTV film a 250 nm thin polyvinylphenol (PVP) layer is spin coated. The PVP layer is used as gate dielectric and also as insulator for the second level of interconnect. This second level and the gate electrodes are defined in the top PANI layer using the second mask.

Stack-integrity is a requirement throughout the whole process; dissolution or physical change of

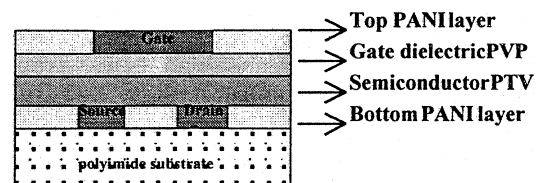


Fig. 5. Cross section of an all-polymer thin film transistor.

previously deposited layers must be prevented. Hence, for the PTV precursor a solvent is chosen which does not dissolve the structured bottom PANI layer. PTV itself is insoluble in common organic solvents and the PVP dielectric is made insoluble by cross-linking [5,6]. Finally, the inverted geometry of the transistors having a top common gate electrode prevents degradation of the PTV semiconductor by deep UV irradiation, see Fig. 5.

Transistors with channel lengths down to 2 μm are routinely obtained and even functional 1 μm transistors have been fabricated. Electrical characteristics of a transistor with a channel length of 2 μm and a channel width of 1 mm are presented in Fig. 6.

The PMOS transistors operate in accumulation mode. The channel is already enhanced at 0 V bias; i.e. they are “normally ON” devices. Hysteresis is clockwise and may be due to charge trapping in the PVP gate dielectric. The resulting threshold voltage shift is one of the reliability issues that are presently being investigated. Other issues include shelf- and operational lifetime. Limited preliminary data show that shelf lifetime may depend on the ambient: the presence of water sometimes is detrimental. The operational lifetime varies from seconds to hours. Current saturation is clearly observed at higher drain voltage. The charge carrier mobility is $3 \times 10^{-4} \text{ cm}^2/\text{V s}$ at a gate voltage of -10 V . This mobility is dependent on the gate voltage. Combining several transistors into

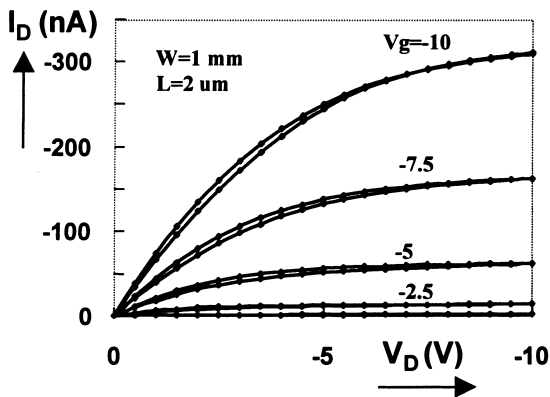


Fig. 6. I - V characteristics of all-polymer thin film transistor.

integrated circuits requires the use of vertical interconnects (vias) between (bottom) source and drain electrodes of one transistor and the (top) gate electrode of another transistor. A simple mechanical technique for the fabrication of the vertical interconnects is used. Sharp pins are punched through overlapping contact pads defined in top and bottom electrode layers. Removal of the pins results in holes in the film and in a local intimate mixing of the top and bottom PANI electrodes. Complete foils with large quantities of vertical interconnects are made using an automated process with the third mask containing information on the position of the vias. The contact resistance typically is 3 k Ω for each via.

Transistors were combined into simple test circuits such as inverters and 2-input NAND gates. In the design the property that the field-effect transistors are already enhanced at 0 V gate-source bias is used. Therefore, the load transistor (see Fig. 7) can act as a constant current source.

Transfer characteristics for these test circuits with channel lengths down to 2 μm show voltage amplification. Hence, they are successfully coupled into 7-stage ring oscillators. The oscillators operate at supply voltages as low as 3 V. Their operating frequency typically is 40–200 Hz, and is dominated [4] by the RC time constant of the load transistors of the logic gates.

In more complex circuits the basic cells are limited to single input inverters and 2-input NAND gates. Similarly, the channel length was

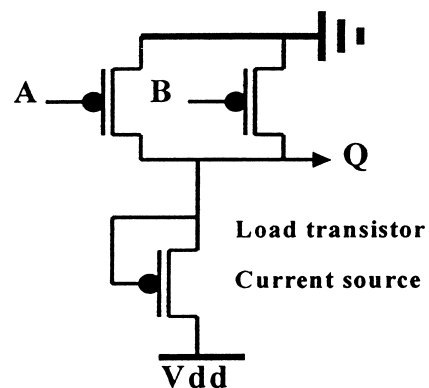


Fig. 7. Schematic of a 2-input NAND gate.

chosen as 5 μm to order to get maximum robustness against spread in individual transistor parameters.

As an example D-type flip-flops were constructed of 2-input NAND gates and successfully operated in a divide-by-2 arrangement.

To demonstrate the ability to fabricate functional integrated a 15-bit mechanically programmable code generator was made. A micrograph of part of it is shown in Fig. 8. The channel widths are 0.2 mm and 1 mm for the driver and load transistors respectively. The black spots in Fig. 8 are the mechanically made vias. The width of the interconnect is 10 μm . The integrated circuit, combining 326 transistors and over 300 vias, consists of an on-board clock generator, a 5 bit counter, decoder logic and 15 programming pads. A large output transistor modulates the supply current according to the programmed pattern. The circuit produces a user (mechanically) programmable serial data stream of 15 bits. A DC voltage is applied and the current through the output transistor is measured. The bit rate obtained is 30 bits/s. The circuits remain functioning when the foils are sharply bent. The code generator can for example be used as a programmable load of a tuned LC circuit, forming an electronic bar code label. The (programmed) serial data stream can then be read at a distance when the label is put in an electromagnetic field at the LC-resonance fre-

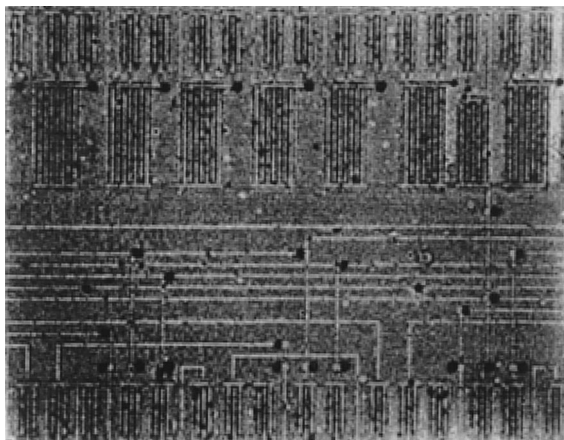


Fig. 8. Micrograph of part of the 15-bit code generator.

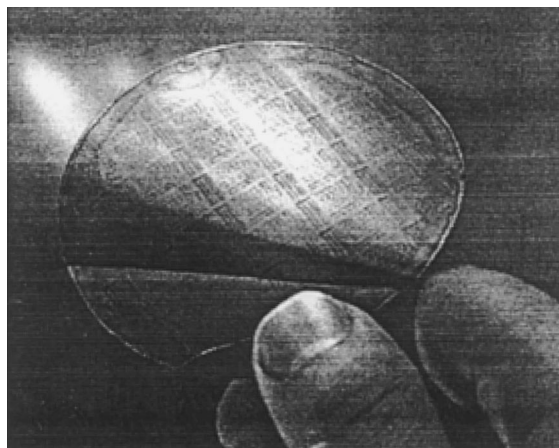


Fig. 9. Photograph of a 3" polyimide foil containing the all-polymer integrated structures.

quency [6,7]. Note that the field also provides the label with the necessary supply voltage. A photograph of a finished foil, presented in Fig. 9, shows a flexible substrate containing about 50 identical dies. Each die contains a variety of components and electronic test circuits for characterization and modeling as well as one 15-bit programmable code generator. These integrated circuits are visible as the high-density rectangles.

5. Summary

In summary, the electrical properties of two solution-processed organic semiconductors (pentacene and PTV) were investigated and a model was presented to describe the gate-voltage and temperature dependence of the mobility of (amorphous) organic transistors. Furthermore, an improvement of the room temperature mobility by one order of magnitude of both pentacene and PTV was shown to be possible by optimizing the process conditions. Finally, functional all-polymer integrated circuits have been realized using a simple and potentially inexpensive technology. Attention is now focused on further decrease of cost and on increasing the operating frequency by using polymeric semiconductors with higher charge carrier mobility and by scaling down the lateral dimensions.

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